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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/576,312	04/18/2006	Johannus Leopoldus Bakx	NL 031238	9405
24737 7590 06/22/2010 PHILIPS INTELLECTUAL PROPERTY & STANDARDS P.O. BOX 3001 BRIARCLIFF MANOR, NY 10510			EXAMINER CHU, KIM KWOK	
			ART UNIT 2627	PAPER NUMBER
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/576,312	<b>Applicant(s)</b> BAKX, JOHANNUS LEOPOLDUS	
	<b>Examiner</b> Kim-Kwok CHU	<b>Art Unit</b> 2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on Amendment filed on 3/17/2010.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-5 and 8-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5 and 8-17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 April 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                    | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)         | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                          |

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### ***Claim Objections***

1. Claim 1 is objected to because of the following informalities:

Regarding Claim 1, line 17, the phrase "a first detector unit" should be changed to --the first optical detector unit--; and

Regarding Claim 1, line 20, the phrase "a second detector unit" should be changed to --the second optical detector unit--.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

*A person shall be entitled to a patent unless --  
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.*

3. Claims 1-5 and 8-17 are rejected under 35 U.S.C. § 102(b) as being anticipated by Oshima (U.S. Patent 6,445,670).

4. Oshima teaches an optical detector system having all of the elements and means as recited in Claims 1-5, 8-14 and 16. For example, Oshima teaches the following:

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Regarding Claim 1, the optical detector system 104 Fig. 6) comprising at least two optical detector units 125A, 125B (Fig. 7A) for receiving light generated from at least two lasers 115A, 115B, respectively (Fig. 7A; column 13, lines 1 and 2), each optical detector unit 125A, 125B comprising an array of detector segments (Figs. 7A and 8) and at least one output terminal (current paths in substrate) defining a current output of the corresponding optical detector unit (Fig. 7A; column 14, lines 48-50; the optical detector system is an integrated circuit having input/output circuits fabricated in a common substrate); and a signal processing circuit 109 (Fig. 6; column 14; lines 50-54); wherein at least one current output 117 (Fig. 7A; column 14, lines 48-52) of a first optical detector unit 125A is connected directly at a common current output node (substrate 117 is a common current path such as a ground path) to a corresponding current output of a second optical detector unit 125B (117 (Figs. 7A); the output node 117 (ground path in substrate) being directly connected to a processing terminal of the signal processing circuit 109 (Fig. 6) so that the processing terminal is directly connected to both the at least one current output of the first optical detector unit 125A and the corresponding current output of the second optical detector unit 125B, and wherein only a first optical detector unit 125A

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of the at least two optical detector units 125A, 125B is operative (Fig. 7A; column 13, lines 60-65), as determined by an identity of a first laser 125A in use of the at least two lasers (Fig. 7A), a second optical detector unit 125B of the at least two optical detector units 125A, 125B being non-operative (not active) by virtue of not receiving light from a second laser 115B of the at least two lasers 115A, 115B (Fig. 7A) so that an output of the second optical detector unit 125B (Fig. 7A) is floating (off), and does not affects output signals produced by the first optical detector unit 125A (Fig. 7A; each set of laser light and it corresponding detector is activate to their respective disc).

Regarding Claim 2, the two optical detector units 125A, 125B Fig. 7A) are of mutually identical design (Fig. 7A; same semiconductor material).

Regarding Claim 3, the two optical detector units 125A, 125B have mutually different wavelength sensitivity ranges (Fig. 6; two laser 115A and 115B).

Regarding Claim 4, each current output of the first optical detector unit 125A is connected directly to the corresponding current output of the second optical detector unit 125B at a corresponding output node 117 (Fig. 7A; two detectors belongs to the same substrate).

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Regarding Claim 5, the second optical detector unit 125B in the non-operative state presents a high input impedance (Fig. 7A; no signal/current flowing).

Regarding Claim 8, the signal processing circuit 109 has at least one input terminal connected via a conductor (Fig. 6; column 12, lines 51-53) to a corresponding output node of the optical detector system 104, and wherein the at least one input terminal comprises a current input (Figs. 6 and 7A; inherent feature where input/output circuits such as 109 carries current in form of a signal).

Regarding Claim 9, the signal processing circuit 109 has at least one input terminal connected via a conductor (Fig. 6; column 12, lines 51-53) to a corresponding output node of the optical detector system 104, the one input terminal comprises a voltage input, and wherein a terminator resistor is connected to the line (Fig. 7A; inherent feature where input/output circuits use terminator resistors to limit currents).

Regarding Claim 10, the terminator resistor is arranged in the proximity of the signal processing circuit 109 (Fig. 6; inherent feature where input/output circuits use terminator resistors to limit currents).

Regarding Claim 11, the terminator resistor is integrated in an IC implementing the signal processing circuit 109 (Fig. 6;

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inherent feature where input/output circuits use terminator resistors to limit currents).

Regarding Claim 12, light beam generating means 115A, 115B for generating at least two light beams (Fig. 6); optical components 107 (Fig. 6) for directing and focusing the two light beams in a focal spot on an optical disc 81A, 82B (Fig. 6); optical components 107 (Fig. 6) for directing reflected light beams to respective optical detector units 125A, 125B of the optical detector system (Figs. 6 and 7A).

Regarding Claim 13, the optical components 107 are arranged such that the light beams have at least partly common light paths (Fig. 6; both light beams focused).

Regarding Claim 14, the optical components 107 are arranged such that the light beams have completely separate light paths (Fig. 7A; only one light beam is on).

Regarding Claim 16, the disc drive apparatus comprising an optical system 105, 106 107, 108 (Fig. 6).

5. Claims 15 and 17 have limitations similar to those treated in the above rejection, and are met by the reference as discussed above.

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***Response to Remarks***

6. Applicant's Amendment and Remarks filed on March 17, 2010 have been fully considered. Applicant does not agree that the prior art of Oshima (U.S. Patent 6,445,670) teaches "at least one current output of a first optical detector unit is connected directly at a common output node to a corresponding current output of a second optical detector unit" (page 1 of the Remarks, lines 11-15). Accordingly, the prior art of Oshima teaches an integrated circuit 104 (Fig. 6) having two photo-detectors 125A and 125B (Fig. 7A; column 14, lines 45-53). The two photo-detectors receive reflected light beams and then convert the monitored light beams into corresponding currents. In order to send the currents to the matrix computation means 109 (Fig. 6), the photo-detectors 125A and 125B use circuit paths as current transmission means. Since the two photo-detectors are built on a single substrate, their circuit paths connected to the matrix computation means 109 must have a same common point. This common point can be a current ground loop, a voltage group loop or a common input of the matrix computation 109. In other words, it is not necessary that the matrix computation 109 uses two separate connecting points to the photo-detectors 125A and 125B because only one of the photodetector is functioning at any time. On the other hand,



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even the two photo-detectors are outputting currents to the matrix computation 109, their current grounds are a common point.

Furthermore, Applicant states that the prior art of Oshima does not teach "output node being directly connected to a processing terminal of the signal processing circuit" (page 1 of the Remarks, lines 17-19). Accordingly, in Fig. 6, the prior art of Oshima teaches that the optical unit 104 which containing two photo-detectors 125A and 125B (Fig. 7A) is connected to a matrix computation means 109 for signal processing.

**7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).**

**A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.**

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8. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Kim CHU whose telephone number is (571) 272-7585 between 9:30 am to 6:00 pm, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoa Nguyen, can be reached on (571) 272-7579.

The fax number for the organization where this application or proceeding is assigned is (571) 273-8300

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished application is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9191 (toll free).

/Kim-Kwok CHU/

Examiner AU2627  
June 9, 2010  
(571) 272-7585  
/HOA T NGUYEN/

Supervisory Patent Examiner, Art Unit 2627